REMARKS

Claims 1-12 are currently pending in this application. Claims 1-12 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 1-12 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,005,812 (Mullarkey).

As an initial matter, although the Examiner has acknowledged that Claims 13-21 were cancelled, the Examiner has maintained his rejection of Claim 13 (c.f., Office Action, Pages 2 and 5).

Regarding the Examiner's rejection under 35 U.S.C. 112, first paragraph, of Claims 1-12, the specification and FIG. 4 have been amended to comply with the Examiner's recommendations. FIG. 4, as attached hereto, has been amended such that it is in accordance with the amended specification. Accordingly, withdrawal of the rejection under 35 U.S.C. §112, first paragraph, of Claims 1-12 is respectfully requested. No new matter has been added.

Regarding the Examiner's rejection under 35 U.S.C. 112, second paragraph, of Claim 1, Claim 1 has been amended to overcome the Examiner's rejection. Accordingly, withdrawal of the rejection under 35 U.S.C. §112, second paragraph, of Claim 1 is respectfully requested.

Regarding the rejection of independent Claim 1 under §102(b), the Examiner states that Mullarkey anticipates all of the elements of the claim. More specifically, the Examiner equates

the reference voltage, as recited in Claim 1, with the output of inverter 27 (shown in FIG. 2 of Mullarkey) and equates the at least one voltage level, as recited in Claim 1, with Vccp as taught by Mullarkey.

Mullarkey discloses a device and method for supplying current to a semiconductor memory to support boosted voltage within the memory during testing. Only one reference voltage (i.e., Vccp) is ever generated by the device disclosed by Mullarkey. In other words, Mullarkey merely teaches controlling a single voltage output Vccp.

Moreover, with reference to FIG. 2 of Mullarkey, it is clearly seen that the signal output from inverter 27 is a logic signal which merely has an assertion that is opposite to the logic level of the Test signal (which the Examiner equates with the clock control signal as recited in Claim 1). Therefore, the signal output from inverter 27 is merely $\overline{TEST}$ as opposed to a reference voltage.

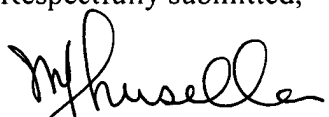
Additionally, in an Office Action issued in the parent application (i.e., U.S. Patent Application No. 10/118,253—which issued into U.S. Patent No. 6,083,805 B2) and dated October 23, 2003, at page 4, the Examiner asserted "to attempt to read the applied reference to Mullarkey on claim 21 would require reading the 'reference voltage' and the [at least] 'one voltage' as both being Vccp, which would be improper." It is further noted that the at least one voltage and the reference voltage, as recited by Claim 1, of the present application corresponds with the at least one voltage and the reference voltage, as recited by Claim 1, of U.S. Patent Application No. 10/118,253.

Accordingly, as Mullarkey does not teach or suggest each and every limitation of Claim 1, it is respectfully requested that the rejection under 35 U.S.C. §102(b) of Claim 1 be withdrawn.

In light of the discussion above, it is respectfully submitted that independent Claim 1 overcomes the stated rejection and is in condition for allowance. Without conceding the patentability per se of dependent Claims 2-12, it is respectfully submitted that these claims are also in condition for allowance by virtue of their dependence on Claim 1.

Claims 1-12 are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or a personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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